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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	08/838,452
Filing Date	04/07/1997
First Named Inventor	WARREN FARNWORTH
Art Unit	2829
Examiner Name	KARLSEN, E.
Attorney Docket Number	91-62.17

Total Number of Pages in This Submission

ENCLOSURES *(Check all that apply)*

- [x] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
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- [ ] Information Disclosure Statement
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- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
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- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
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- [ ] After Allowance communication to Technology Center (TC)
- [ ] Appeal Communication to Board of Appeals and Interferences
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- [ ] Proprietary Information
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Stephen A. Gratton, Reg. No. 28,418 THE LAW OFFICE OF STEPHEN A. GRATTON
Signature	
Date	April 12, 2004

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FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 330.00

Complete if Known	
Application Number	08/838,452
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First Named Inventor	WARREN M. FARNWORTH
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METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☒ Deposit Account:

Deposit Account Number: 07-1857

Deposit Account Name: Stephen A. Gratton

The Director is authorized to: *(check all that apply)*

☒ Charge fee(s) indicated below ☐ Credit any overpayments

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

		Extra Claims		Fee from below	Fee Paid
Total Claims		-20** =		X	=
Independent Claims		- 3** =		X	=
Multiple Dependent					=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	330
1402	330	2402	165	Filing a brief in support of an appeal	
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 330

SUBMITTED BY

(Complete *(if applicable)*)

Name (Print/Type)	Stephen A. Gratton	Registration No. (Attorney/Agent)	28,418	Telephone	303 989 6353
Signature				Date	4/12/2004

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

WARREN M. FARNWORTH
ALAN G. WOOD
TRUNG TRI DOAN
DAVID R. HEMBREE

Art Unit: 2829

Serial No.: 08/838,452

Filing Date: 04/07/1997

Examiner: Karlsen, E.

Title: TEST APPARATUS FOR TESTING SEMICONDUCTOR DICE INCLUDING SUBSTRATE WITH PENETRATION LIMITING CONTACTS FOR MAKING ELECTRICAL CONNECTIONS (AS AMENDED)

Attorney Docket No.: 91-62.17

APPELLANT'S BRIEF (37 CFR 1.192)

April 12, 2004

Mail Stop Appeal Brief - Patents
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

This Brief is submitted in triplicate to the Board of Patent Appeals and Interferences, and is being filed concurrently with a Notice of Appeal dated 04/12/2004. This Brief is accompanied by the requisite fee under a separate transmittal.

The Brief and Notice of Appeal are in response to the final rejections contained in the final Office Action dated 01/13/2004. The claims under appeal are listed in Appendix I.

1. REAL PARTY IN INTEREST

The real party in interest in the appeal is Micron Technology, Inc., the assignee of record of the patent application.

2. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences that will directly affect, or be directly affected by, or have a bearing on the Board's decision in this appeal.

3. STATUS OF CLAIMS

Claims 1-77, 84-86, 89 and 95 have been canceled.

Claims 83 and 94 have been withdrawn from consideration.

Claims 78-82, 87, 88, 90-93 and 96-98 have been rejected under 35 USC §112, second paragraph, as being indefinite. The 35 USC §112, second paragraph, rejections of claims 78-82, 87, 88, 90-93 and 96-98 is being appealed.

Claims 78-82, 87, 88, 90-93 and 96-98 have been rejected under 35 USC 103(a) as being unpatentable over Enochs (US Patent No. 4,597,617) in view of Nakano (JP Hei 3-69131) and Blonder et al. (US Patent No. 4,937,653) or Agahdel et al. (US Patent No. 5,402,077). The 35 USC §103(a) rejections of claims 78-82, 87, 88, 90-93 and 96-98 is being appealed.

4. STATUS OF AMENDMENTS

No amendments have been filed subsequent to the final rejections.

5. SUMMARY OF INVENTION

The appealed claims are directed to an apparatus ***(burn-in fixture 11-Figure 8)*** for testing a semiconductor die ***(die 21-Figure 6)*** having a plurality of pads ***(bondpads***

27-Figure 6). The apparatus includes a plate ***(die cavity plate 13-Figure 8)*** for retaining the die, a substrate ***(substrate 41-Figure 6)*** configured to make temporary electrical connections with the die ***(die 21-Figure 6),*** and a biasing member ***(elastomeric strip 83-Figure 8)*** configured to bias the die ***(die 21-Figure 6)*** against the substrate ***(substrate 41-Figure 6)*** with a biasing force.

The substrate ***(substrate 41-Figure 6)*** includes contacts ***(bumps 61-Figure 6)*** with raised portions ***(raised portions 73-Figure 6)*** for penetrating the pads ***(bondpads 27-Figure 6)*** on the die ***(die 21-Figure 6)*** to a self limiting penetration depth. The contacts ***(bumps 61-Figure 6)*** are constructed such that a biasing force with which the biasing member ***(elastomeric strip 83-Figure 8)*** presses the die ***(die 21-Figure 6)*** and the substrate ***(substrate 41-Figure 6)*** together is sufficient to cause the raised portions ***(raised portions 73-Figure 6)*** on the contacts ***(bumps 61-Figure 6)*** to penetrate the pads ***(bondpads 27-Figure 6)*** on the die ***(die 21-Figure 6)***. This is the lower limit of the biasing force. At the same time, the biasing force is selected to be less than a force required for the remaining portions of the contacts ***(bumps 61-Figure 8)*** to penetrate the pads ***(bondpads 27-Figure 6)*** on the die ***(die 21-Figure 6)***. This is the upper limit of the biasing force.

Appendix II is a Claim Chart reading the appealed claims on the specification and drawings.

6. ISSUES

A first issue is whether claims 78-82, 87, 88, 90-93 and 96-98 are indefinite under 35 USC §112, second paragraph.

A second issue is whether claims 78-82, 87, 88, 90-93 and 96-98 are unobvious under 35 U.S.C. 103(a) over Enochs (US Patent No. 4,597,617) in view of Nakano (JP Hei 3-69131) and Blonder et al. (US Patent No. 4,937,653) or Agahdel et al. (US Patent No. 5,402,077).

Appendix III includes copies of the references cited in the 35 USC §103 rejections.

7. GROUPING OF CLAIMS

The following groups of claims are deemed to separately stand or fall together.

Group I - Claims 78-82.

Group II - Claims 87-88 and 90-91.

Group III - Claims 92-93 and 96.

Group IV - Claims 97-98.

8. ARGUMENT

REJECTIONS UNDER 35 USC §112, second paragraph

The 35 USC §112, second paragraph rejections are based in part on the term "biasing member" in independent claims 78, 87, 92 and 97. In regard to these rejections the final Office Action mailed 01/13/2004 states:

> "All of the claims are considered functional in that they do not include sufficient structure to provide the stated function. The clams all call for a stack of elements including a plate, a substrate and a biasing member. The biasing member is argued by Applicants to be element 83 of Applicants' disclosure. Element 83 is a layer of elastomeric material. The biasing member is claimed in the claims to be configured to bias the contacts of the substrate and the pads of a die together with a force. Where the biasing member is just a layer it cannot have a

function of biasing. Maybe it could bias as a result of its weight. The disclosed apparatus presumably could be used in any orientation in a gravitational field but presumably the plate would normally be "under" the substrate and the biasing member. It is noted that Applicants' biasing is actually provided by pressure created by clamp 89 which squeezes the plate, substrate and biasing member together. The biasing member 83 cannot provide biasing on its own and attributing biasing to it alone goes beyond its function."

However, it is accepted that a claim can omit information that would be obvious to a person of ordinary skill in the art. In re Skrivan, 427 F.2d 801, 166 USPQ 85 (CCPA 1970). Similarly, it is not necessary that a claim recite each and every element needed for the practical utilization of the claimed subject matter. Bendix Corp. v United States, 600 F.2d 1364, 204 USPQ 617 (Ct. Cl 1979).

Thus if an inventor claims an appliance having an electric motor, it is not necessary to claim the electrical cord on the appliance which carries electric power to the motor. Some elements of an invention are obvious to one skilled in the art, and the absence of these elements does not render the claim indefinite or misdescriptive under §112, second paragraph. See also, In re Anderson, 471 F.2d 1237, 176 USPQ 331 (CCPA 1973); In re Geerdes, 491, F.2d 1260, 180 USPQ 789 (CCPA 1974); In re Cook, 439 F.2d 730, 169 USPQ 298 (CCPA 1971); Ex parte Vollheim, 191 USPQ 407 (POBA 1976).

In the present case the biasing member 83 (Figure 8) operates with a cover 15 (Figure 8) and a clamp 89 (Figure 8) to hold it in place. However, the cover 15 (Figure 8) and the clamp 89 (Figure 8) are known in the art, as exemplified by US patent application serial no. 8/46,675 cited on page 23, lines 12-16 of the specification. Other

elements such as threaded fasteners and a plate, rather than the clamp 89 (Figure 8) and the cover 15 (Figure 8), could alternately be used to hold the biasing member 83 in place.

Appellant also disputes the Examiner's contention that the clamp 89 (Figure 8) generates the biasing force and the biasing member 83 does not generate the biasing force. In this regard, the plate 15 (Figure 8) presses against the die cavity plate 13 (Figure 8), so that the biasing force for making electrical contact between the die 21 (Figure 8) and the substrate 41 (Figure 8) is generated by the resiliency of the biasing member 83 (Figure 8). The biasing member 83 is in effect a spring which generates a force independent of its weight.

The 35 USC §112, second rejections are also based in part on the recitation of the "biasing member on the plate" and the "substrate on the plate". In this regard the final Office Action mailed 01/13/2004 states:

"The claims are further confusing for stating that a first element is "on" a second element when there is an intervening element. For instance in claim 78 and other claims the substrate is stated to be on the plate and the biasing member is stated to be "on" the plate. In reality the biasing member is on the plate and the substrate is on the biasing member."

In the present claims, the "plate" refers to the die cavity plate 13 (Figure 8), which is the base element on which other elements of the apparatus are mounted. It is common practice in apparatus claims, to recite a base element, and than to recite other elements of the apparatus as being "on" the base element. Further, the occurrence of intermediate elements between an element and the base element, does not mean the element is not "on" the base element. For example, a rider is referred to as being "on"

a horse, even if a saddle is present between the rider and the horse. Although the saddle is an intermediate element, the recitation of the rider being on the horse is still definitive.

Similarly, the "on" recitation would also be clear to one skilled in the art in the interpretation of the present claims. Admittedly, the "on" recitation is broader than the "under" recitation suggested by the Examiner (page 2, line 15 of the final Office Action mailed 01/13/2004). However, "If the metes and bounds of a claimed invention are clearly ascertainable, then the claim, no matter how broad, cannot be property rejected as "vague and indefinite" under the language of the second paragraph of §112." In re Gardner, 427 F.2d 786, 166 USPQ 138 (CCPA 1970); In re Goffe, 526 F.2d 1393, 188 USPQ 131 (CCPA 1975)."

REJECTIONS UNDER 35 USC §103 (a)

Appellant submits that the 35 USC §103 rejections are in error, and that the present claims are unobvious over the prior art. As a first argument, Appellant submits the claims are unobvious because they include limitations not taught or suggested by the prior art. As a second argument, Appellant submits that one skilled in the art at the time of the invention would have no incentive to combine the references in the manner of the Office Action.

The criteria of MPEP 2142, 2143 on establishing obvious are thus not met by the rejections. Specifically, MPEP 2142, 2143 states as follows:

"First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success

in obtaining the claimed invention based upon the references relied upon by the Examiner. Third, the prior art reference (or references when combined) must teach or suggest all the claim limitations."

First Argument - Claim Limitations Not Taught Or Suggested By Prior Art

The present invention is directed to a "test apparatus for testing a semiconductor die having a plurality of pads". Test apparatus for semiconductor dice were developed in the early 1990s by semiconductor manufacturers to test and certify singulated semiconductor dice as known good dice (KGD). Specifically, singulated dice can be temporarily housed in these test apparatus, then burn in tested at elevated temperatures in a burn in oven. The passing dice could then be packaged, or used individually in bare form. Prior to that time, dice were tested at the wafer level, particularly with probe cards, but were not burn in tested until after packaging. If a packaged die was determined to be defective after burn in testing, the packaging costs were wasted.

However, with prior art test apparatus, problems can occur during testing, because the contacts on the test apparatus damage the dice. In particular, in order to make good electrical connections with the dice a large biasing force needs to be exerted between the dice and mating contacts on the test apparatus. This problem is compounded because each test apparatus is a self contained unit, that is used many times to test dice having different physical characteristics, such as pad height and planarity. Accordingly, the biasing force was oversized even more to insure reliable electrical connections.

The present test apparatus includes a substrate with contacts having a self limiting penetration depth. In addition, the present test apparatus relates the self limiting structure of the contacts to the biasing force applied by an internal biasing member. Specifically, the raised portions (73-Figure 6) of the contacts (61-Figure 8)

penetrate the pads (27-Figure 6) on the die (21-Figure 6) at the selected biasing force, while the remainder of the contacts (e.g., the flat surfaces on the bump 61 in Figure 6) provide a stop plane for limiting further penetration. Damage to the die is thus limited, and the upper and lower limits of the biasing force can be quantified. In addition, the biasing member (elastomeric strip 83-Figure 8) can be constructed to achieve this biasing force.

Appellant submits that the feature of a penetration limiting contacts in combination with a biasing member is not taught or suggested by the cited art. This feature is recited in each independent claim (claims 78, 87, 92 and 97). Appellant further submits that the feature of relating the biasing force applied by the biasing member to the structure of the penetration limiting contacts is not taught or suggested by the cited art. This feature is also recited in each independent claim.

Independent claim 78 relates the biasing force to the structure of the penetration limiting contacts by reciting "the bump dimensioned to limit further penetration of the raised portions into the pad at the force". Independent claim 87 relates the biasing force by reciting "the force selected to be greater than a first force at which the points penetrate the pad but less than a second force at which the remainder of the bump penetrates the pad". Independent claim 92 recites "the force selected to be greater than a first force at which the raised portions penetrate the pad but less than a second force at which the bump penetrates the pad". Independent claim 97 recites the "force selected to achieve penetration of the pad by the points to the penetration depth".

These different force recitations in the independent claims make the each grouping of claims separately patentable. In addition, independent claims 78 and 92 state that the bumps include "spaced raised portions",

whereas independent claims 87 and 97 state the bumps include "spaced points".

The 35 USC §103 rejections are based on the combination of Enochs, in view of Nakano, and Blonder et al., or Agahdel et al.

In citing Enochs the final Office Action mailed 01/13/2004 states:

"Enochs shows the basic combination of claimed elements. Element 24 is a plate that includes a plurality of external leads 28. Element 34 is a substrate with a surface and contacts on the surface. Element 32 is a biasing member on the plate. Enochs does not show a substrate of semiconductor material and contacts each of which comprise a bump with raised portions."

Enochs is directed to a "package for connecting an integrated circuit chip to an etched circuit board (col. 1, lines 39-40), rather than to a "test fixture for testing a semiconductor die" as presently claimed. The package includes a base 10, an etched circuit board 24 on the base 10, a flex circuit 34 on the circuit board 24 having posts 34, a silicone pressure pad 32, and a top plate 16. As shown in Figure 3 of Enochs, assembly of the package forms a compressed stack in which the posts 42 on the flex circuit 34 electrically engage bond pads on an IC circuit chip 52 (column 4, lines 27-35 of Enochs).

In addition to not being a test apparatus, Enochs does not disclose or suggest a penetration limiting contact, whose operation is related to an internally generated biasing force. Because they are not penetration limited, the posts 34 in Enochs could damage the bondpads on the IC circuit chip 52.

Nakano has been cited by the Examiner as teaching a penetration limiting contact. As stated in the final Office Action mailed 01/13/2004:

"Nakano shows in Figures 1a and 1b a semiconductor substrate 10 having bumps 21 with a raised portion 22 where

the raised portion is coated with metal. Nakano does not show a plurality of raised portions."

Although Nakano et al. teaches a penetration limiting contact, there is no suggestion of using this type of contact with a biasing member in the presently claimed type of testing apparatus. In addition, there is no suggestion of relating a biasing force applied by the biasing member to the structure of the penetration limiting contact. Specifically, Nakano et al. is directed to a probe card, such that the biasing force for biasing the contact with the wafer is externally generated by something other than a biasing member configured as presently claimed (e.g., movement of the wafer or the probe card by a hydraulic cylinder or a press). The biasing force on a probe card can be precisely ascertained and controlled, and does not need to be oversized as in the present test apparatus.

Another deficiency of the Nakano et al. contact is that only a single raised portion 22 per bump 21 is employed. In independent claims 78, 87, 92 and 97 plural penetrating structures are recited. The advantage of the plural penetrating structures is that they can be smaller for preventing damage to the pads on the dice. In addition, the plural penetrating structures spread current out over a larger area of the pads on the die. This helps to prevent overheating of the pads due to high current density over a small area.

To supplement Nakano et al., Blonder et al. was cited as teaching plural raised points on a contact structure. However, Blonder et al. teaches permanent, rather than temporary electrical connections, as in the presently claimed test apparatus. Specifically, Blonder et al. teaches a permanent connection system that requires "bonding of the carrier pads to the chip pads" (col. 2, lines 40-41). Further, Blonder et al. does not relate contact force to penetration depth. Rather as explained in

column 4, lines 49-55 of Blonder et al., an external mechanical pressure is applied to the chips and carrier. Again this pressure can be mechanically controlled, and a special contact structure to limit the penetration depth, as a function of contact pressure is not required.

As Blonder et al. teaches plural points in the context of bonded connections there is no suggestion of penetration limitation, as a function of biasing force applied by a biasing member in a test apparatus.

Agahdel et al. was also cited as teaching contact pads 40 (Figure 4) having plural penetrating particles 44 (Figure 4) projecting from the contact pads 40. One of the particles 44 is shown in Figure 5 of Agahdel et al. As stated at column 6, lines 34-36 of Agahdel:

"The particle 44 is embedded in a layer of hard metal 46 (such as nickel or tungsten) which binds the particle to the contact pad 40."

These particles 44 in Agahdel et al. would not have the same height, as with the bumps and raised portions that form the presently claimed contacts. Rather, the particles 44 would project from the pads 40 with a random height, such that the pads 40 would have an irregular surface and a variable height on the polymer layer 39. The present bumps are uniform and precise structures, which as stated in each independent claim have "a height" on the surface of the substrate. As shown in Figure 6 of the present application, one benefit of the uniform height of the bumps 61 is that the die 21 is spaced from the surface 49 of the substrate 41 by a uniform distance, which is approximately equal to the height of the bumps 61. In addition, the raised portions 73 are part of the bumps 61, such that a unitary structure is provided and fabrication is simplified.

Agahdel et al. teaches at column 2, lines 46-49:

"It also includes a mechanism for adjusting the force with which the die is pressed against the interconnect circuit in order to ensure adequate electrical contact without causing damage."

However, Agahdel et al. also does not teach that the pads 40 and the particles 44 have a structure related to a force applied by a biasing member.

Second Argument - No Incentive To Combine Cited References

Appellant would further argue that there is no incentive in the references, or in the prior art, for combining the references in the manner of the rejections.

In this regard, Enochs is directed to a package rather than to a test apparatus, and Nakano et al. is directed to a probe card, such that there would be no incentive to include their teachings in a test apparatus. Blonder et al. is directed to permanently bonded connections, such that there would be no incentive to include it's teachings in a test apparatus. Agahdel et al. is the only cited reference that teaches a test apparatus. However, there is no suggestion of a penetrating limiting contact in combination with an internal biasing member.

In regard to the motivation to combine the references, the final Office Action mailed 01/13/2004 states:

"It would have been obvious to one of ordinary skill in the art at the time of the invention to have adapted the plural raised portion feature of Blonder et al. or Agahdel et al. to the resulting combination because one skilled in the art would realize that so doing would result in better contact with less damage to the pads being contacted."

In combining the references, the motivation for the combination must be from the view point of one skilled in the art at the time of the present invention, and without the benefit of the present disclosure. However, the

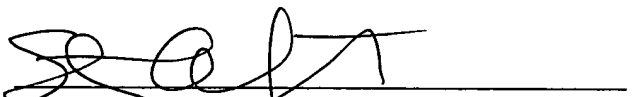
"better contact" and "less damage" motivation, while in the present disclosure is not taught or suggested by the cited art. In addition, there is no suggestion in the cited art of combining a penetration limiting contact having multiple penetration points, with a biasing member constructed to relate biasing force to the structure of the contact.

Conclusion

In view of the above arguments, Appellant submits the rejections of claims 78-82, 87, 88, 90-93 and 96-98 are not proper. Appellant thus requests the rejections be reversed, and the claims be allowed.

DATED this 12th day of April, 2004.

Respectfully submitted:



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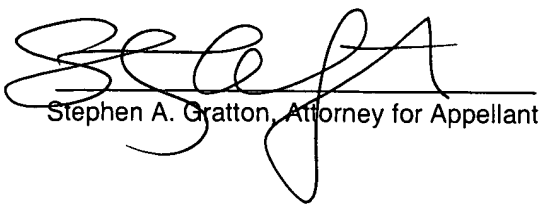
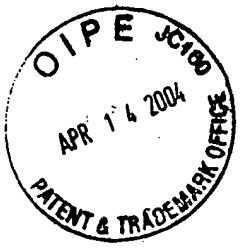


Stephen A. Gratton, Attorney for Appellant



Appendix I
Appellant's Brief
Serial No. 08/838,452

Appealed Claims

78. An apparatus for testing a semiconductor die having a plurality of pads comprising:

a plate;

a substrate on the plate comprising a surface and a plurality of contacts on the surface configured to electrically contact the pads; and

a biasing member on the plate configured to bias the contacts and the pads together with a force;

the plate, the substrate and the biasing member configured such that the die can be placed on the substrate and biased against the substrate with the contacts in electrical contact with the pads;

each contact comprising a bump on the substrate having a height on the surface and a plurality of raised portions dimensioned to penetrate into a pad to a penetration depth less than a thickness of the pad, the bump dimensioned to limit further penetration of the raised portions into the pad at the force.

79. The apparatus of claim 78 wherein the bump is dimensioned to penetrate into the pad at a second force which is greater than the force.

80. The apparatus of claim 78 further comprising a plurality of conductive traces on the substrate in electrical communication with the contacts, and a plurality of external leads on the plate in electrical communication with the traces.

81. The apparatus of claim 78 wherein the substrate comprises silicon and the bump comprises metal.

82. The apparatus of claim 78 wherein the pads comprise bondpads.

87. An apparatus for testing a semiconductor die having a plurality of pads comprising:

a plate comprising a plurality of external leads;

a substrate on the plate comprising a surface and a plurality of contacts on the surface configured to electrically contact the pads; and

a biasing member on the plate configured to bias the contacts and the pads together with a force;

the plate, the substrate and the biasing member configured such that the die can be placed on the substrate and biased against the substrate with the contacts in electrical contact with the pads;

each contact comprising a bump on the substrate having a height on the surface and a plurality of spaced points on the bump configured to penetrate into a pad with a penetration depth less than a thickness of the pad while a remainder of the bump limits further penetration, the force selected to be greater than a first force at which the points penetrate the pad but less than a second force at which the remainder of the bump penetrates the pad.

88. The apparatus of claim 87 wherein the substrate comprises silicon and the bump comprises metal.

90. The apparatus of claim 87 wherein the bump comprises a second surface and the raised portions project from the second surface.

91. The apparatus of claim 87 further comprising a plurality of conductive traces on the substrate and a plurality of bond pads on the conductive traces.

92. An apparatus for testing a semiconductor die having a plurality of pads comprising:

a plate;

a substrate on the plate comprising a surface and a plurality of contacts on the surface configured to electrically contact the pads; and

a biasing member on the plate configured to bias the contacts and the pads together with a force;

the plate, the substrate and the biasing member configured such that the die can be placed on the substrate and biased against the substrate with the contacts in electrical contact with the pads;

each contact comprising a bump having a height on the surface and a plurality of spaced raised portions dimensioned to penetrate into a pad at the force by a penetration depth less than a thickness of the pad while the bump limits further penetration into the pad, the force selected to be greater than a first force at which the raised portions penetrate the pad but less than a second force at which the bump penetrates the pad.

93. The apparatus of claim 92 further comprising a plurality of external leads on the plate in electrical communication with the contacts.

96. The apparatus of claim 92 wherein the raised portions comprise points.

97. An apparatus for testing a semiconductor die having a pad with a thickness comprising:

a plate;

a substrate on the plate comprising a surface and a contact on the surface configured to electrically contact the pad, the contact comprising a bump having a height on the surface, and a plurality of points comprising portions of the bump projecting therefrom, the points configured such that the points can penetrate into the pad to a penetration depth less than the thickness while a remainder of the bump limits further penetration into the pad; and

a biasing member on the plate configured to bias the die and the substrate together with a force selected to achieve penetration of the pad by the points to the penetration depth.

98. The apparatus of claim 97 wherein the substrate comprises silicon and the bump comprises metal.

Appendix II

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Claim Chart

78. An apparatus	**burn-in fixture 11 first described on page 13, lines 9-10 and shown in Figures 1 and 2, also described as an "apparatus" at page 1, line 10**
for testing a semiconductor die	**die 21 first described on page 13, line 13 and shown in Figure 6**
having a plurality of pads	**bondpads 27 first described on page 13, line 14 and shown in Figure 6**
comprising:	
a plate;	**die cavity plate 13 first described on page 13, line 10 and shown in Figure 8**
a substrate	**substrate 41 first described on page 14, lines 8-10 and shown in Figure 6**
on the plate	**die cavity plate 13 first described on page 13, line 10 and shown in Figure 8**
comprising a surface	**surface 49 first described on page 16, line 23 of the specification and shown in Figure 6**

and a plurality of contacts	**bumps 61 first described on page 17, line 19 and shown in Figure 6, and also described as alternate embodiments of the die contacts 43 on page 16, lines 7-8**
on the surface	**surface 49 first described on page 16, line 23 of the specification and shown in Figure 6**
configured to electrically contact the pads; and	**page 14, lines 11-12**
a biasing member on the plate	**elastomeric strip 83 shown in Figure 8 and described as a "biasing member" at page 21, line 17**
configured to bias the contacts and the pads together with a force	**antecedent basis for "force" on page 17, line 27 and page 21, line 3**
the plate,	**die cavity plate 15 shown in Figure 8**
the substrate	**substrate 41 shown in Figure 6**
and the biasing member	**elastomeric strip 83 shown in Figure 8**
configured such that the die can be placed on the substrate and biased against the substrate with the contacts in electrical contact with the pads	**page 17, lines 1-3 and page 14, lines 10-12**
each contact comprising a bump	**bump 61-Figure 6**

on the substrate	**substrate 41-Figure 6**
having a height	**page 9, lines 7-8**
on the surface	**surface 49**
and a plurality of raised portions	**raised portions 73 first described on page 17, line 20 and shown in Figure 6**
dimensioned to penetrate into a pad to a penetration depth less than a thickness of the pad,	**page 17, line 21 and page 18, lines 1-3**
the bump dimensioned to limit further penetration of the raised portions into the pad at the force.	**page 17, lines 25-30 and page 9, lines 12-15**

79. The apparatus of claim 78 wherein the bump is dimensioned to penetrate into the pad at a second force which is greater than the force. **page 17, lines 25-30**

80. The apparatus of claim 78 further comprising a plurality of conductive traces on the substrate in electrical communication with the contacts, **conductive traces 45 first described on page 14, lines 14-15 and shown in Figure 6**

and a plurality of external leads on the plate in electrical communication with the traces. **external connector leads 33 first described on page 13, line 20 and shown in Figure 8**

81. The apparatus of claim 78 wherein

the substrate comprises silicon	**page 14, line 14**
and the bump comprises metal.	**page 16, line 8**

82. The apparatus of claim 78 wherein the pads comprise bondpads.	**bondpads 27 first described on page 13, line 14**
87. An apparatus	**burn-in fixture 11 first described on page 13, lines 9-10 and shown in Figures 1 and 2, and described as an "apparatus" at page 1, line 10**
for testing a semiconductor die	**die 21 first described on page 13, line 13 and shown in Figure 6**
having a plurality of pads	**bondpads 27 first described on page 13, line 14 and shown in Figure 6**
comprising:	
a plate	**die cavity plate 13 first described on page 13, line 10 and shown in Figure 8**
comprising a plurality of external leads;	**external connector leads 33 first described on page 13, line 20 and shown in Figure 8**
a substrate	**substrate 41 first described on page 14, lines 8-10 and shown in Figure 6**
on the plate	**die cavity plate 13 first described on page 13, line 10 and shown in Figure 8**
comprising a surface	**surface 49 first described on page 16, line 23 of the specification and shown in Figure 6**
a plurality of contacts on the surface	**bumps 61 first described on page 17, line 19 and shown in**

	Figure 6, and also described as alternate embodiments of the die contacts 43 on page 16, lines 7-8
configured to electrically contact the pads; and	**page 14, lines 11-12**
a biasing member on the plate	**elastomeric strip 83 shown in Figure 8 and described as a biasing member on page 21, line 17**
configured to bias the contacts and the pads together with a force;	**antecedent basis for force on page 17, line 27 and page 21, line 3**
the plate,	**die cavity plate 15 shown in Figure 8**
the substrate	**substrate 41 shown in Figure 6**
and the biasing member	**elastomeric strip 83 shown in Figure 8**
configured such that the die can be placed on the substrate and biased against the substrate with the contacts in electrical contact with the pads	**page 17, lines 1-3 and page 14, lines 10-12**
each contact comprising a bump	**bump 61-Figure 6**
on the substrate	**substrate 41-Figure 6**
having a height on the surface	**page 9, lines 7-8**
and a plurality of spaced points	**raised portions 73 shown in Figure 6 and described as points on page 9, line 9**

on the bump	**bump 61-Figure 6**
configured to penetrate into a pad with a penetration depth less than a thickness of the pad while a remainder of the bump limits further penetration,	**page 17, line 21 and page 18, lines 1-3**
the force selected to be greater than a first force at which the points penetrate the pad but less than a second force at which the remainder of the bump penetrates the pad.	**page 17, lines 25-30 and page 9, lines 12-15**
88. The apparatus of claim 87 wherein the substrate comprises silicon	**page 14, line 14**
and the bump comprises metal.	**page 16, line 8**
90. The apparatus of claim 87 wherein the bump comprises a second surface and the raised portions project from the surface.	**surface of bump 61 with raised portions 73 shown in Figure 6**
91. The apparatus of claim 87 further comprising a plurality of conductive traces	**conductive traces 45 first described on page 14, lines 14-15 and shown in Figure 6**
and a plurality of bond pads on the conductive traces.	**substrate bondpads 47 first described on page 14, line 15 and shown in Figure 6**
92. An apparatus	**burn-in fixture 11 first described on page 13, lines 9-10 and shown in Figures 1 and 2, and described as an "apparatus" at page 1, line 10**

for testing a semiconductor die	**die 21 first described on page 13, line 13 and shown in Figure 6**
having a plurality of pads	**bondpads 27 first described on page 13, line 14 and shown in Figure 6**
comprising:	
a plate;	**die cavity plate 13 first described on page 13, line 10 and shown in Figure 8**
a substrate	**substrate 41 first described on page 14, lines 8-10 and shown in Figure 6**
on the plate	**die cavity plate 13 first described on page 13, line 10 and shown in Figure 8**
comprising a surface	**surface 49 first described on page 16, line 23 and shown in Figure 6**
a plurality of contacts on the surface	**bumps 61 first described on page 17, line 19 and shown in Figure 6, and also described as alternate embodiments of the die contacts 43 on page 16, lines 7-8**
configured to electrically contact the pads;	**page 14, lines 11-12**
and a biasing member on the plate	**elastomeric strip 83 shown in Figure 8 and described as a "biasing member" at page 21, line 17**
configured to bias the contacts and the	

pads together with a force;	**antecedent basis for force on page 17, line 27 and page 21, line 3**
the plate,	**die cavity plate 15 shown in Figure 8**
the substrate	**substrate 41 shown in Figure 6**
and the biasing member	**elastomeric strip 83 shown in Figure 8**
configured such that the die can be placed on the substrate and biased against the substrate with the contacts in electrical contact with the pads	**page 17, lines 1-3 and page 14, lines 10-12**
each contact comprising a bump	**bump 61-Figure 6**
on the substrate	**substrate 41-Figure 6**
having a height on the surface	**page 9, lines 7-8**
and a plurality of spaced raised portions dimensioned to penetrate into a pad at the force by a penetration depth less than a thickness of the pad while the bump limits further penetration into the pad,	**page 17, line 21 and page 18, lines 1-3**
the force selected to be greater than a first force at which the raised portions penetrate the pad but less than a second force at which the bump penetrates the pad.	**page 17, lines 25-30 and page 9, lines 12-15**

93. The apparatus of claim 92 further comprising a plurality of external leads on the plate in electrical

communication with the contacts.	**external connector leads 33 first described on page 13, line 20 and shown in Figure 8**
96. The apparatus of claim 92 wherein the raised portions comprise points.	**raised portions 73 shown in Figure 6 and described as points on page 9, line 9**
97. An apparatus	**burn-in fixture 11 first described on page 13, lines 9-10 and shown in Figures 1 and 2, and described as an "apparatus" at page 1, line 10**
for testing a semiconductor die	**die 21 first described on page 13, line 13 and shown in Figure 6**
having a pad	**bondpads 27 first described on page 13, line 14 and shown in Figure 6**
with a thickness	**page 18, lines 1-3**
comprising:	
a plate;	**die cavity plate 13 first described on page 13, line 10 and shown in Figure 8**
a substrate	**substrate 41 first described on page 14, lines 8-10 and shown in Figure 6**
on the plate	**die cavity plate 13 first described on page 13, line 10 and shown in Figure 8**
comprising	

a surface	**surface 49 first described on page 16, line 23 of the specification and shown in Figure 6**
and a contact on the surface configured to electrically contact the pad, the contact comprising a bump	**bumps 61 first described on page 17, line 19 and shown in Figure 6, and also described as alternate embodiments of the die contacts 43 on page 16, lines 7-8**
having a height,	**page 9, lines 7-8**
on the surface	**surface 49 first described on page 16, line 23 of the specification and shown in Figure 6**
and a plurality of points comprising portions of the bump projecting therefrom,	**raised portions 73 shown in Figure 6 and described as points on page 9, line 9**
the points configured such that the points can penetrate into the pad to a penetration depth less than the thickness while a remainder of the bumps limit further penetration into the pad;	**page 17, lines 19-30 and page 9, lines 12-15**
and a biasing member on the plate	**elastomeric strip 83 shown in Figure 8, and described as a "biasing member" on page 21, line 17**

configured to bias the die and the substrate together with a force selected to achieve penetration of the pad by the points to the penetration depth.

page 17, lines 25-30 and page 18, lines 1-3

98. The apparatus of claim 97 wherein the substrate comprises silicon

page 14, line 14

and the bump comprises metal.

page 16, line 8

Appendix III

Appellant's Brief
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REFERENCES CITED IN 35 USC §103 REJECTIONS

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(54) Title of the Invention: **A Probe for Testing Semiconductor Integrated Circuits and a Test Method Using Said Probe**
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1. **[Title of the Invention] A Probe for Testing Semiconductor Integrated Circuits and a Test Method Using Said Probe.**

2. **[Limits of the Patent Claims]**
[Claim 1] A semiconductor integrated circuit test probe which is characterized by provision of a semiconductor substrate, by formation of multiple needle-shaped protuberances upon one surface of said semiconductor substrate surface by selective etching, by electrical isolation of the respective needle-shaped protuberances from each other by an isolation method, and by connection of said needle-shaped protuberances to an external circuit by a beam lead structure.

[Claim 2] A semiconductor integrated circuit test probe per Claim 1 characterized by selective etching of the surface of said semiconductor substrate to form multiple protuberances, said protuberances having a flat surface.

[Claim 3] A method for manufacture of a semiconductor device, said method being characterized by inclusion of a step which performs characteristic testing while contacting said needle-shaped protuberances of the previously mentioned test probe of Claim 1 and Claim 2 to the pads formed upon the wafer or chip

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containing the semiconductor integrated circuit being tested.

3. **[Detailed Explanation of the Invention]**

[Summary] This invention pertains to a test probe for use in the testing of wafer or chip semiconductor integrated circuits. One surface of a semiconductor substrate is selectively etched to form multiple needle-shaped protuberances upon said semiconductor substrate (the respective protuberances being electrically isolated from each other by an isolation process) and a means for contacting said needle-shaped protuberances to an external circuit via a beam lead structure, with the goal of making highly reliable contact with the pads arrayed upon a high density integrated circuit, said pads being on the order of 10 μm across.

[Field of Industrial Application] This invention pertains to a test probe for use during the testing of wafer or chip semiconductor integrated circuits.

[Prior Art] The processes for manufacture of a semiconductor integrated circuit may be roughly divided into the procedures that form semiconductor circuits within regions of the chip or wafer, the processes that divide the resultant wafer into separate chips, and processes that end in the completion of the individual chip packages. Static and dynamic characteristic testing is performed upon the wafer integrated circuits that were formed during these processes. Integrated circuits are selected for subsequent processing after these characteristic tests. A test probe containing multiple metallic probe needles is made to temporarily electrically connect the above mentioned integrated circuit to an external test circuit (signal generator, power source, etc.) to perform these characteristic tests.

Figure 6 shows the structure of the prior art probe used for the above mentioned tests. As shown in Figure 6 (a), multiple probe needles 3, made from tungsten, are fixed to the top surface of a printed circuit board provided with a central aperture roughly 30 mm in diameter. Palladium and beryllium/copper are also used for these probe needles 3. As shown in Figure 6 (b), the tip of each probe needle 3 is bent so as to protrude toward the bottom surface of the printed circuit board through aperture 2. The position of the far end of respective probe needles 3 corresponds to the location of pads provided upon the integrated circuit chip. Such pads, for example, may be spaced 200 μm apart in a square pattern. The opposite end of probe needle 3 is contiguous with interconnects 4 upon printed circuit board 1 which connect to board contacts 5.

During testing one integrated circuit region upon the wafer is aligned within the central hole 2. Then the tips of probe needles 3 are pushed into contact with the various pads provided at the periphery of the integrated circuit chip. Test signals and electrical power voltage are supplied via board contacts 5.

[Problems that the Invention is to Solve] The above mentioned prior art test

probe has two major problems:

(1) When the tips of probe needles 3 are pushed against the integrated circuit chip 11 pads, as shown in Figure 7, rubbing against the pads 11 occurs in the lateral direction. Item 3, drawn with dashed lines, shows the probe needle 3 prior to the occurrence of lateral movement. This movement may easily result in damage to pad 11, which is constructed from aluminum, etc. Such pad damage may result in problems during the subsequent bonding process. In particular bonding may become impossible when the ball-bonding method is used for the connections between integrated circuit chip 10 and the external circuitry.

(2) Since the tips of the multiple tungsten, etc. probe needles extend several centimeters from their fixed ends, it is difficult to assure precise placement upon the tested integrated circuit chip pads, which are spaced roughly 200 μm apart. Moreover, it is difficult to say if the mechanical strength of the probe needles is sufficient since the tip of probe needle 3 must mechanically collide with and may get caught upon the tested circuit, resulting in probe needle tip deformation.

Also as the density of semiconductor integrated circuits is increased, the number of connections with the external circuitry increase. Therefore the surface area upon the integrated circuit covered by pads increases. Therefore it becomes necessary that the pad surface area and spacing should be reduced so that the fraction of the surface occupied by pads does not increase.

It is relatively easy to reduce the surface area and spacing of the pads upon the integrated circuit. Although dimensional control is possible on the order of a micron, placing the prior art test probe needles 3, as shown in Figure 6, with sufficient degree of dimensional precision is a problem. It has been difficult to accomplish such testing using the prior art test probe.

This invention provides a test probe which can solve the above mentioned problems of the prior art. Moreover the goal of this invention is to make possible testing of large scale integrated circuits using such a test probe.

[Means for Solution to the Problems] This invention achieves the above goals by providing a semiconductor integrated circuit test probe which is characterized by provision of a semiconductor substrate, by formation of multiple needle-shaped protuberances upon one surface of said semiconductor substrate surface by selective etching, by electrical isolation of the respective needle-shaped protuberances from each other by an isolation method, and by connection of said needle-shaped protuberances to an external circuit by a beam lead structure.

Also this invention is a semiconductor integrated circuit test probe as per Claim 1 characterized by selective etching of the surface of said semiconductor

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substrate to form multiple protuberances, such protuberances having a flat surface. Also this invention is a method for manufacture of a semiconductor device, said method being characterized by inclusion of a step which performs characteristic testing while contacting said needle-shaped protuberances of the previously mentioned test probe to pads upon the wafer chip containing the semiconductor integrated circuit being tested.

[Operation of the Invention] The contacts used for the test probe of this invention are formed by the small scale fabrication techniques established for semiconductor integrated circuit manufacture. An array consisting of multiple minute closely spaced needle-shaped protuberances are formed simultaneously.

Specifically:

(1) Needle-shaped protuberances are formed upon a semiconductor substrate by anisotropic etching of the semiconductor crystal.

(2) The respective contacts are formed isolated electrically from each other by use of the techniques such as those used during semiconductor integrated circuit manufacture for isolation of circuit elements.

(3) One type of semiconductor integrated circuit bonding technology that may be used to connect the respective contacts to an external circuit is the beam lead method.

Therefore it becomes possible to effectively conduct characteristic testing of large scale integrated circuits using this test probe, as was previously done with the prior technology for less dense circuits. The probe of this invention may be used to examine large scale integrated circuits upon a wafer, even when the tested integrated circuit chip pad spacing and size are so small as to require high precision placement of test probe contacts. Furthermore since the tips of all of the test probe contacts are within the same plane, it is no longer necessary to use additional pressure against the pads of the tested integrated circuit to assure uniform contact. Also damage, as was seen with the prior art test probe to the tested integrated circuit pads, is lessened since lateral movement does not occur.

[Embodiments of the Invention] Below the invention is explained while referring to illustrations.

Figure 1 shows a partial diagram of the test probe of this invention for testing semiconductor integrated circuits. Silicon chip 10 has the same size as the tested semiconductor integrated circuit. Upon one surface of silicon chip 10 are formed multiple contacts by an etching process. The tips of respective probe contacts 11 have a needle shape and are placed so as to correspond one-to-one to the positions of pads upon the tested integrated circuit. The respective probe

contacts 11 are electrically isolated from each other by means that will be explained later.

Upon silicon chip 10 are provided means for connection to an external circuit. For example, such means might be a structure such as beam lead electrodes 12, a well-known method. Within the center of silicon chip 10 is provided a visual observation window 14. This visual observation window 14 is used to perform alignment of the tested integrated circuit chip and the test probe of this invention.

Probe contacts 11 are formed into a cone shape by an etching process. These cones bite into the aluminum metal pads as the test probe is pushed against the pads of the integrated circuit chip during testing. Therefore damage is possible when contact pressure is increased such that the contact breaks through the pad metal layer to the insulation and dopant-containing layers of the semiconductor substrate beneath. To avoid this problem and to simplify the test procedure, it is advantageous to use probe contacts constructed as shown in Figure 2 (a).

In other words, needle-shaped protuberances 22 are formed above multiple planar protuberances 21 by selective etching of silicon chip 10. As shown in Figure 2 (b). The planar surface of contact 20 of Figure 2 (a) butts up against the pad 25 formed upon the tested integrated circuit chip 24 when the test probe is pressed against the tested integrated circuit chip 24. By this means deep scoring of pad 25 by probe contact 22 is prevented.

The method of manufacture of the test probe of this invention is explained while referring to Figure 3.

One side of a silicon wafer is oxidized. After the SiO_2 layer is formed, the SiO_2 layer is etched using well-known lithography techniques. SiO_2 mask layer 31 spots 20 μm in diameter are formed upon the previously mentioned silicon wafer 30 surface. Figure 3 (b) shows the cross section indicated by X-X within Figure 3 (a). The spacing of the SiO_2 mask layer 31 spots is the same as the pads upon the (unillustrated) integrated circuit chip under testing. For example, these SiO_2 mask layer 31 spots may be spaced 40 μm apart.

Next the silicon wafer 30 is etched around the SiO_2 mask layer 31 to a depth 10 μm using, for example, a well-known mixed isotropic etchant solution containing nitric and hydrofluoric acids. During this etching process silicon wafer 30 is etched in the vertical direction as well as beneath the SiO_2 layer mask spots in the lateral direction due to the side etching effect. Since the mass of silicon removed by this side etching increases as the distance from the original silicon wafer surface decreases, as the surface is etched to a depth of 10 μm, needle-shaped protuberances 32 are left behind beneath the SiO_2 mask layer 31 spots, as shown in Figure 3 (c). The height of the needle-shaped protuberances

32 is roughly 10 μm.

A <100> crystal orientation silicon wafer 30 is used. The etching rate depends upon crystal orientation. For example, an etchant solution such as KOH may be used to form needle-shaped protuberances 32 by isotropic etching. It is also possible to form non-cone-shaped needle-shaped protuberances 32. Also it is possible to deposit beforehand a doped silicon layer 10 μm thick upon the silicon wafer 30 so as to easily control the etched mass and hence shape of the needle-shaped protuberances 32. Such a dopant-containing surface layer could be formed upon the silicon wafer 30 surface by epitaxial growth.

It is possible to form the probe contacts 20 shown in Figure 2 by first forming needle-shaped protuberances 22 and then placing resist layer over protuberances 21, which include the needle-shaped protuberances 22. The uncovered silicon wafer surface then undergoes anisotropic etching.

After the remnant SiO_2 mask layer 31 is removed, a SiO_2 layer is formed upon the silicon wafer 30 surface by thermal oxidation. The surface is coated with resist. Then this resist layer is exposed and developed. As shown in Figure 3 (d), an opening is formed in the resist coating, This opening in the resist 35 includes needle-shaped protuberances 32 as well as the neighboring contact regions 34. Figure 3 (e) shows a cross-sectional view of the Y-Y transect indicated in Figure 3 (d). Item 36 is the previously mentioned SiO_2 layer. The pattern of resist mask 35 covers the 10 μm step region which includes needle-shaped protuberance 32. It is also possible to use an exposure method other than positive resist / e-beam exposure.

Next the remnant resist is removed to leave SiO_2 layer 36 as a mask. Dopant is diffused into the remaining clear silicon wafer surface 30 of the needle-shaped protuberances 32 as well as contact regions 34. This dopant would be n-type if silicon wafer 30 is p-type. As a result as shown in Figure 3 (f), the surface of needle-shaped protuberances 32 as well as contact regions 34 becomes a n-type region 38.

Then as indicated by Figure 3 (g) (top view) and cross-sectional diagram Figure 3 (h), electrode 39 is formed in contact with contact region 34. Electrode 39 my be formed from gold, for example. As explained later, the electrode may be connected to external circuitry using the well-known beam lead structure. Also to prevent alloy formation between the silicon wafer 30 and the gold electrode 39, a barrier metal layer is formed between electrode 39 and silicon wafer 30. It is necessary that electrode 39 should be formed sufficiently shorter than needle-shaped protuberance 32 above the test probe surface so that contact is not made with the test integrated circuit chip during testing.

Next silicon wafer 30 is divided into separate test probe chips. For example during this separation process, the entire needle-shaped protuberance 32

containing surface of silicon wafer 30 is covered by resist, while on the back side of the silicon wafer, the region corresponding to the test probe is covered with resist. The unmasked silicon wafer 30 may be removed by etching so as to open the previously mentioned observation window 14 (Figure 1), so that observation window 14 is formed simultaneous to the division of the silicon wafer into test probe chips.

The test probe of this invention, shown in Figure 3 (i), is formed in the above mentioned manner. Electrodes 39 are formed extending laterally along the entire test probe to form a beam lead structure.

The above mentioned test probe of this invention is fixed to a printed circuit board 1, such as that shown in Figure 7 for the prior art test probe. It is permissible to bond electrode 39 to connector 4. Another mounting technique is to fix the test probe chip into a recess within ceramic substrate 40, as shown in Figure 4, and then to bond electrodes 39 to connections 41. Ceramic substrate 40 is generally stronger than a printed circuit board, easily assuring precise positioning of the test probe as well as a high degree of parallelism between the test probe and the wafer.

In the above mentioned example of the test probe of this invention, the surface of needle-shaped protuberance 32 and the contact region 34 were made to be in electrical contact by the formation of n-type region 38. Therefore if a voltage lower than the range used for test measurements (including the ground) is applied to silicon chip 10, a reverse bias voltage results in the electrical isolation of the respective needle-shaped protuberances 32. It is also possible, for example, to lower the contact resistance of needle-shaped protuberances 32 by covering needle-shaped protuberances 32 with a metallic tungsten or tungsten silicide layer.

It is also possible to electrically mutually isolate needle-shaped protuberances 32 by using an insulation layer. For example, such an electrical insulation structure may be formed by silicon on insulator (SOI) technology. In other words, a SOI 50 is used for test probe fabrication as shown in Figure 5 (a) per the well-known technique. The SOI substrate is formed upon a normal thickness silicon wafer 51 and SiO_2 layer 52. SiO_2 layer 52 is formed upon silicon wafer 51 by thermal oxidation of the wafer surface. Upon this SiO_2 layer 52 is deposited silicon layer 53 by epitaxy at high temperature. The thickness of silicon layer 53 may be later adjusted by chemical mechanical polishing to 12 μm thick, for example. Either the silicon layer may be pre-doped as n-type, or at least the surface layer may be diffusion doped after said polishing step.

Upon this silicon layer 53 surface may be formed needle-shaped protuberances by the same masking procedure as shown in Figure 3. A SiO_2 mask is formed as shown in Figure 5(b). Then needle-shaped protuberances 55 are formed by etching silicon layer 53. Next the remaining silicon layer 53 is

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selectively etched to form separate needle-shaped protuberances 55, as shown in Figure 5 (c). A contact region 56 is provided corresponding to each needle-shaped protuberance 55. A beam lead electrode structure is formed as in the previous working example. Then the silicon wafer is divided into individual chips. The protuberances 55 shown in Figure 5 are electrically isolated from each other by SiO_2 layer 52. Therefore it is not necessary to make provisions for a special reverse bias voltage to be applied to the test probe substrate to isolate the needle-shaped protuberances.

[Results of the Invention] Per this invention a test test probe may be easily made with an array of contacts that correspond to the pads of a high density integrated circuit chip. In comparison to the prior art test probe, these contacts of the test probe of this invention may be positioned with a high degree of accuracy and parallelism with the pads. Also this test probe provided by this invention is more resistant to mechanical collision. Furthermore, damage caused to the pads of the tested integrated circuit chip is decreased, making possible improved production and reliability of high density integrated circuit devices.

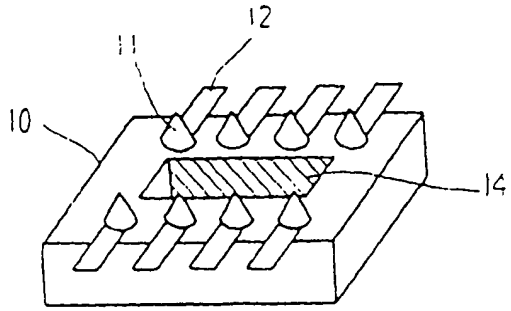

Figure 1. This shows the test probe of this invention.

10. Silicon Chip
11. Probe Contacts
12. Beam Lead Electrodes
14. Visual Observation Window

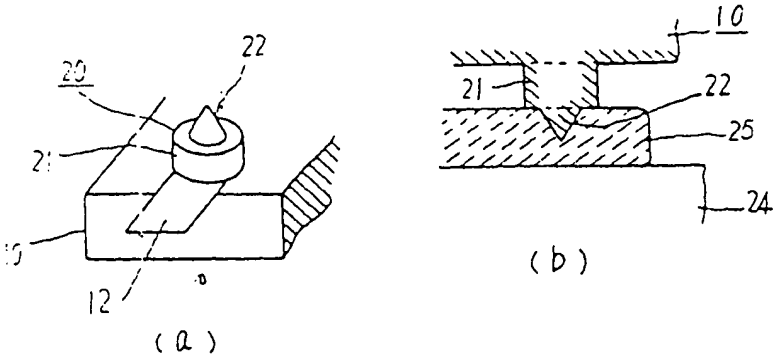

Figure 2. An example of the shape of the probe contact of this invention.

10. Silicon Chip
12. Beam Lead Electrodes
20. Planar Surface
21. Planar Protuberance
22. Probe Contact
24. Integrated Circuit Chip
25. Pad

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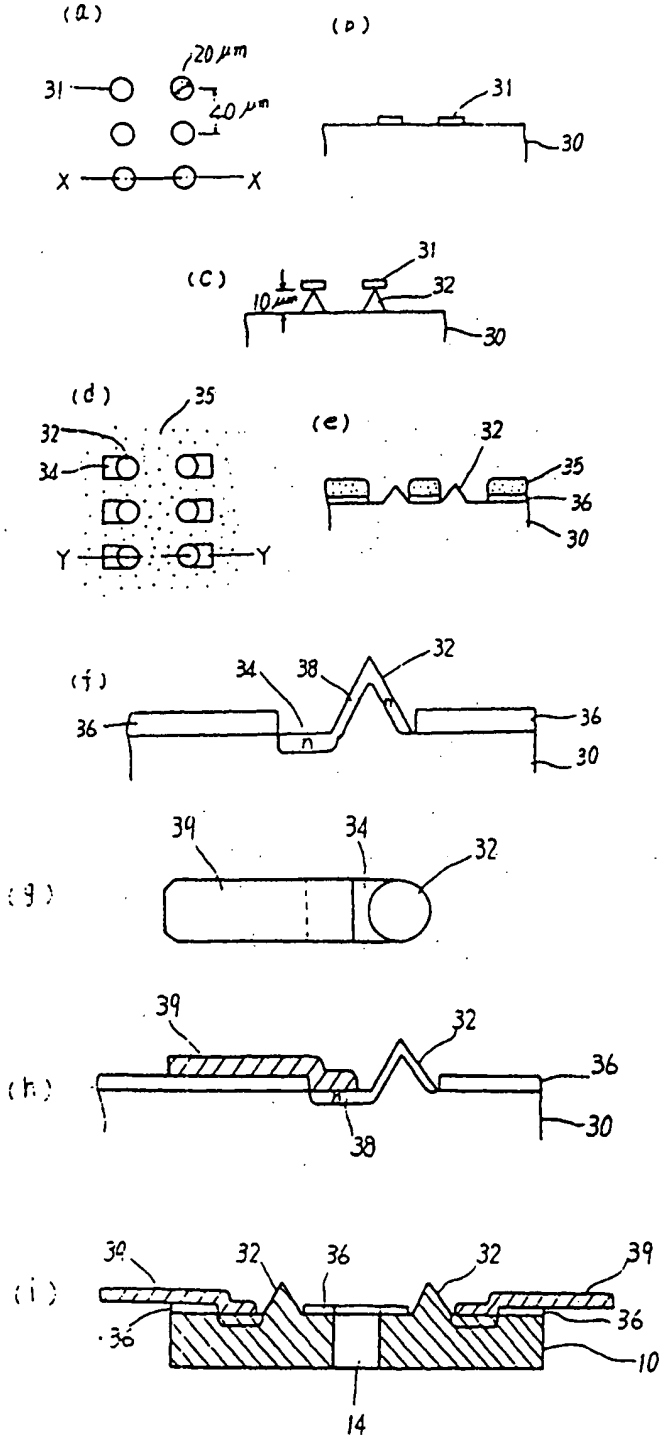

Figure 3. A working example of the construction of the test probe of this invention.

10. Silicon Chip
30. Silicon Wafer
31. SiO_2 Layer
32. Needle-Shaped Protuberance
34. Contact Region
35. Resist
36. SiO_2 Layer
38. n-Type Region
39. Electrode

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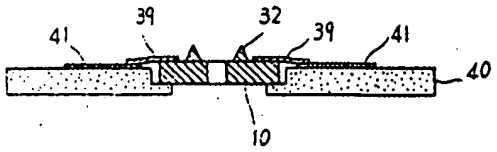

Figure 4. A view of the completed test probe of this invention.

10. Silicon Chip
32. Needle-Shaped Protuberance
39. Electrode
40. Ceramic Substrate
41. Contact

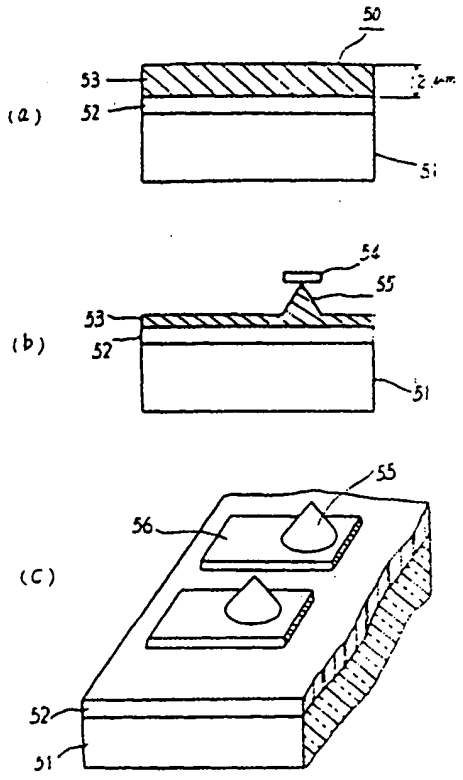

Figure 5. An example of another electrical isolation method for the probe contacts of this invention.

50. Silicon on Insulator
51. Silicon Wafer
52. SiO_2 Layer
53. Silicon Layer
54. Remaining SiO2 Layer
55. Needle-Shaped Protruderance
56. Contact Region

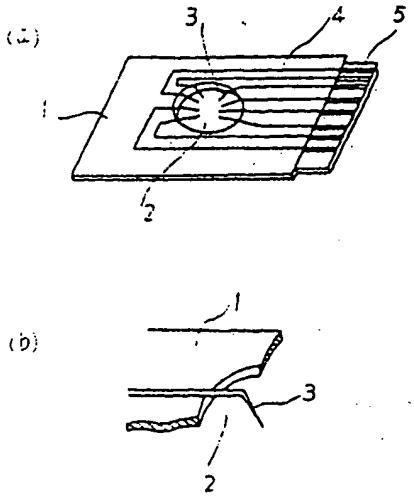

Figure 6. Prior art test probe for testing semiconductor integrated circuits.

1. Printed Circuit Board
2. Aperture
3. Probe Needle
4. Interconnects
5. Board Contacts

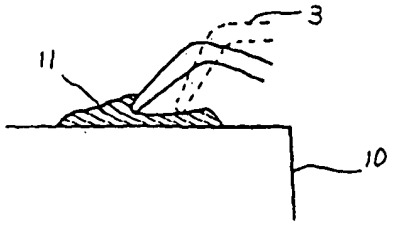

Figure 7. Diagram explaining deficiences of the prior art test probe.

3. Probe Needle
10. Integrated Cricuit Chip
11. Pad